ABSTRACT OF THE DISCLOSURE

A memory cell array is constructed by a plurality of sub-arrays which include a plurality of sub-word lines, a plurality of bit lines, a plurality of plate lines and a plurality of memory cell blocks, plural ones of the sub-arrays being arranged in the sub-word line direction, a plurality of sub-row decoders provided between the plurality of respective sub-arrays, for driving the sub-word lines, a main row decoder disposed on one-end side of the plurality of sub-arrays in the sub-word line direction, and a plurality of main-block selecting lines for respectively supplying outputs of the main row decoder to the sub-row decoders. The main-block selecting lines for connecting the main row decoder to the sub-row decoders are formed of the same interconnection layer as the plate lines and metal interconnections used between the memory cells in the cell block.